

U.S. Department of Commerce, Patent and Trademark Office						Attorney Docket No.		Serial No.	
						BP 3247		10/685,136	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						Applicant(s)			
						Joseph B. Rowlands			
						Filing Date		Group	
						October 14, 2003		2182	

  

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
/TQN/	AA	6,185,520	02/06/01	Brown et al.			
↓	AB	6,298,370	10/02/01	Tang et al.			
	AC	6,266,731	07/24/01	Riley et al.			
	AD	6,195,739	02/27/01	Wright et al.			
	AE	6,138,217	10/24/00	Hamaguchi			
	AF	6,128,728	10/03/00	Dowling			
	AG	6,108,739	08/22/00	James et al.			
	AH	6,094,715	07/25/00	Wilkinson et al.			
	AI	6,009,426	12/28/99	Jouenne et al.			
	AJ	5,963,745	10/05/99	Collins et al.			
↓	AK	5,805,590	09/08/98	Gillard et al.			

  

Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
/TQN/	AL	777 179	05/15/02	EP			<input type="checkbox"/>	<input type="checkbox"/>
↓	AM	00/38069	06/29/00	WO			<input type="checkbox"/>	<input type="checkbox"/>
	AN	893 766	01/27/99	EP			<input type="checkbox"/>	<input type="checkbox"/>
	AO	199 07 200	09/02/99	DE				X
↓	AP	920 157	11/26/98	EP				X

  

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
/TQN/	AR	Giorgi et al., "PSCR: A Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Shared-Memory Multiprocessors; IEEE Transactions on Parallel and Distributed Systems; Vol. 10, No. 7, July 1999
↓	AS	European Search Report for EP Application No. 02025691.3 Broadcom Corp.
	AT	Intel "21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller," Hardware Reference Manual, Revision 1.0, October 1998, 219 pages
↓	AU	Tom R. Halfhill, "SiByte Reveals 64-Bit Core for NPUs; Independent MIPS64 Design Combines Low Power, High Performance," Microdesign Resources, June 2000, Microprocessor Report, 4 pages.

  

Examiner	/Tanh Q Nguyen/	Date Considered	04/05/2007
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
/TQN/	AA	5,764,895	06/09/98	Chung				
↓	AB	5,644,753	07/01/97	Ebrahim et al.				
↓	AC	4,788,679	11/29/88	Kataoka et al.				
	AD							
	AE							
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	AG							
	AH							
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	AJ							
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		Document	Date	Country	Class	Subclass	Yes	No
/TQN/	AL	98/15155	04/09/98	WO			<input type="checkbox"/>	<input checked="" type="checkbox"/>
/TQN/	AM	265 636	10/03/86	EP			<input type="checkbox"/>	<input checked="" type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
/TQN/	AR	SiByte, "The Mercurian Processor," <a href="http://sibyte.com/mercurian">http://sibyte.com/mercurian</a> , January 15, 2001, 2 pages.						
↓	AS	SiByte, "Fact Sheet," SB-1 CPU, October 2000, rev. 0.1, 1 page.						
↓	AT	SiByte, "Fact Sheet," SB-1250, October 2000, rev. 0.2, 10 pages.						
↓	AU	Stepanian, SiByte, "SiByte SB-1 MIPS64 CPU Core, Embedded Processor Forum 2000, June 13, 2000, 15 pages.						
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	AK							
Foreign Patent Documents								
							Translation	
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	AM						<input type="checkbox"/>	<input type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
/TQN/	AR	Jim Keller, "The Mercurian Processor: A High Performance, Power-Efficient CMP for Networking," October 10, 2000, 22 pages.						
↓	AS	SiByte, "Target Applications," <a href="http://sibyte.com/mercurian/applications.htm">http://sibyte.com/mercurian/applications.htm</a> , January 15, 2001, 2 pages.						
↓	AT	SiByte, "SiByte Technology," <a href="http://sibyte.com/mercurian/technology.htm">http://sibyte.com/mercurian/technology.htm</a> , January 15, 2001, 3 pages.						
	AU							
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